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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,282	02/25/2002	Andy Glew	42390P11202	7096

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
TRUONG, BAO Q	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,282	GLEW ET AL.	
	Examiner	Art Unit	
	Bao Q. Truong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,13,14,16-18 and 20* is/are rejected.

7)☒ Claim(s) *7,12,15 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. The examiner acknowledges the applicant's submission of Amendment for Application No. 10/084,282 dated on 12 September 2005. At this point, there are 20 claims pending in the application; there are 3 independent claims and 17 dependent claims, all of which are ready for reconsideration by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-11, 13-14, 16-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Glew et al. (U.S. Patent No. 5,778,407).

Referring to claim 1, Glew teaches a method comprising:

dividing a physical address space into a plurality of segments as a memory accessed by using linear/virtual addresses (see figure 1: element 22; and also see Section 7.4 of *Computer Organization & Design* of Hennessy and Patterson);

computing an interim first address from a physical address from the physical address space as using 35^{th}-12^{th} bits of a physical address to "bit-wise and" with a mask value (see column 4: lines 13-30);

computing an interim base value from a base value associated with the physical address as using 39^{th}-12^{th} (base) bits from value of a variable range register to "bit-wise and" with the mask value (see figure 5: element 40 and column 4: lines 13-30);

comparing the interim first address and the interim base value to determine whether the physical address can be validly translate to obtain a translated address (see figure 6A-B and column 4: lines 19-30); and

if the physical address can be validly translated, combining the physical address with an offset value to obtain the translated address (see column 3: lines 18-22).

For the applicant's conveniences of understanding the examiner's position, the examiner provides Section 7.4 of *Computer Organization & Design* of Hennessy and Patterson wherein physical address space is divided into multiple segments to be accessed with linear or virtual addresses.

As to claim 2, Glew further teaches determining a memory type of the translated address (see figure 5: element 40 and column 5: lines 14-16).

As to claim 3, Glew further teaches reading the memory type from the base value associated with the physical address (see figure 5: element 40 and column 3: lines 47-51, lines 57-63).

As to claim 4, Glew further teaches:

wherein computing the interim first address comprises determining which bits of the physical address should be retained in the interim first address for comparison with the interim base value as using 35^{th}-12^{th} bits of a physical address to "bit-wise and" with a mask value (see column 4: lines 13-30); and

wherein computing the interim base value comprises determining which bits of a base value should be retained in the interim base value for comparison with the interim first address as using 39^{th}-12^{th} (base) bits from value of a variable range register to "bit-wise and" with the mask value (see figure 5: element 40 and column 4: lines 13-30).

As to claim 5, Glew further teaches determining which bits of the physical address and which bits of the base value should be retained for comparison comprises applying a mask value to each of the physical address and the base value, the mask value associated with the physical address (see column 3: lines 57-63 and column 4: lines 13-30).

As to claim 6, Glew further teaches combining comprises:

determining which bits of the physical address should be retained in the translated address as the high order bits of the physical address being the translated portion of the high order bits of a linear address (see column 3: lines 13-18); and

substituting bits from the offset value for bits of the physical address which are not to be retained in the translated address (see column 3: lines 18-22).

As to claims 8-9, Glew further teaches issuing a fault alert as issuing a logic value of "zero" for the match signal if the physical address "and" the mask does not match the base "and" the mask (see figure 6B and column 4: lines 13-30). This means no mapping exists for the physical address to a particular memory type.

As to claims 10-11, Glew teaches using translation lookaside buffer (TLB) to translate memory access address (see figures 2 and 3A). Steps of issuing a notice that an attempt has been made to access a particular segment and detecting whether a fault bit has been set for the particular segment are **inherently** included.

For the applicant's conveniences of understanding the examiner's position, the examiner provides Section 7.4 of *Computer Organization & Design* of Hennessy and Patterson. In *Computer Organization & Design*, the TLB is described to have portion to store valid bits for memory pages/segments (see figure7.22, page 584). If the valid bit for a segment is of, page fault occurs (see Page Faults, page 585).

Referring to claim 13, Glew discloses an apparatus comprising:

a memory having a first address space divided into a plurality of segments as a memory accessed by using linear/virtual addresses (see figure 1: element 22; and also see Section 7.4 of *Computer Organization & Design* of Hennessy and Patterson);

comparison logic circuitry (see figure 6B) coupled to the memory to create an interim first address from a first address from one of the plurality of segments as using 35^{th}-12^{th} bits of a physical address to "bit-wise and" with a mask value (see column 4: lines 13-30), to create an

interim base value as using 39^{th}-12^{th} (base) bits from value of a variable range register to "bit-wise and" with the mask value (see figure 5: element 40 and column 4: lines 13-30), and to compare the interim first address and the interim base value to determine whether the first address belongs to a segment that can be validly translated to obtain a second address (see figure 6A-B and column 4: lines 19-30); and

combination logic circuitry (see figure 3A) coupled to the comparison logic circuitry and to the memory, the combination logic circuitry to combine the first address with an offset value to obtain the second address if the combination logic circuitry indicates that the first address can be validly translated (see column 3: lines 18-22).

As to claim 14, Glew further discloses that the comparison logic circuitry comprises:

masking circuitry to apply a mask value to the first address to obtain the interim first address and to apply the mask value to a base value to obtain the interim base value, the mask value associated with the first address (see figure 6B).

As to claim 16, Glew further discloses a fault detection circuitry coupled to the comparison logic circuitry, the fault detection circuitry to detect and issue fault alerts as issuing a logic value of "zero" for the match signal if the physical address "and" the mask does not match the base "and" the mask (see figure 6B: element 56 and column 4: lines 13-30).

Referring to claim 17, Glew discloses a system comprising:

a processor (see figure 1: element 11 and figures 2 & 4);

a memory having a first address space divided into a plurality of segments as a memory accessed by using linear/virtual addresses (see figure 1: element 22; and also see Section 7.4 of *Computer Organization & Design* of Hennessy and Patterson);

comparison logic circuitry (see figure 6B) coupled to the memory to create an interim first address from a first address from one of the plurality of segments as using 35^{th}-12^{th} bits of a physical address to "bit-wise and" with a mask value (see column 4: lines 13-30), to create an interim base value as using 39^{th}-12^{th} (base) bits from value of a variable range register to "bit-wise and" with the mask value (see figure 5: element 40 and column 4: lines 13-30), and to compare the interim first address and the interim base value to determine whether the first address belongs to a segment that can be validly translated to obtain a second address (see figure 6A-B and column 4: lines 19-30); and

combination logic circuitry (see figure 3A) coupled to the comparison logic circuitry and to the memory, the combination logic circuitry to combine the first address with an offset value to obtain the second address if the combination logic circuitry indicates that the first address can be validly translated (see column 3: lines 18-22).

As to claim 18, Glew further discloses that the comparison logic circuitry comprises:

masking circuitry to apply a mask value to the first address to obtain the interim first address and to apply the mask value to a base value to obtain the interim base value, the mask value associated with the first address (see figure 6B).

As to claim 20, Glew further discloses a fault detection circuitry coupled to the comparison logic circuitry, the fault detection circuitry to detect and issue fault alerts as issuing a logic value of "zero" for the match signal if the physical address "and" the mask does not match the base "and" the mask (see figure 6B: element 56 and column 4: lines 13-30).

Response to Arguments

4. Applicant's arguments, filed on 12 September 2005 with respect to the rejections of claims 1, 13, and 17, have been fully considered but are moot in view of the new ground(s) of rejection as indicated above.

Allowable Subject Matter

5. Claims 7, 12, 15, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (571) 272-4202. The examiner can normally be reached on Monday-Friday from 7:00 AM to 4:00 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Bao Que Truong

BT

Patent Examiner

03 November 2005

Donald A. Sparks

Supervisory Patent Examiner

Technology Center 2100